A Low Power Wide Linear Output Range Biopotential Amplifier

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***Abstract*—This report summarizes a wide linear output range CMOS biopotential amplifier built for physiological measurement. The proposed amplifier is implemented using the SkyWater 130nm CMOS technology with a 1.8V supply. Comprehensive circuit analyses with transient, input and output range, frequency response, and common mode rejection simulations are performed in the Cadence Design Suite environment.**

***Index Terms*—Biopotential amplifier, gain enhancement switch, physiological measurement frontend, wide linear output range.**

I. Introduction

As healthcare monitoring trends continue to progress toward point-of-care and portable solutions, the demand for efficient, effective, and low power physiological monitoring systems has increased. Some of the most widely utilized noninvasive monitoring techniques require use of biopotential signals, typically acquired via electrodes to a patient's skin. Examples include electrocardiogram (ECG/EKG), electroencephalogram (EEG), bioimpedance (EBI), among others. A critical element of the measurement frontend is the biopotential amplifier that determines the overall performance of the measurement system. For the purposes of this project, we focus on ECG signals to setup our initial requirements. Typically, ECG signal amplitudes vary between 80 μV to 5 mV, as shown in Figure 1 [1].

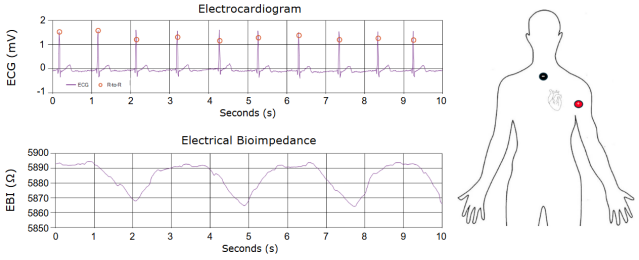

Fig. 1: Example of ECG and EBI signals taken from a live patient.

ECG frequencies range from 0.5 to 100 Hz and are prone to environmental noise such as static, 50/60 Hz power line interference, baseline drift, and inherent skin potentials. To amplify weak and noisy biopotentials without attenuation, amplifiers require stable gain, low noise, high common mode rejection ratio (CMRR), and high input impedance. All of this must be maintained throughout a wide linear output range for the amplifier such that the input range of the ADC is maximized. The linear output range of an amplifier refers to the output range in which the voltage gain remains constant, meaning there is no distortion in the output. A broader linear output range is desirable because a limited range can increase the demands on ADC resolution and power consumption to achieve the necessary signal-to-noise ratio (SNR) in the measurement frontend. The reduction in gain is primarily attributed to variations in the output resistance of the output-stage transistors as the drain-to-source voltage fluctuates. This issue becomes a significant non-ideality, potentially degrading the performance of biopotential amplifiers, especially as transistor sizes shrink and supply voltages decrease further.

II. Circuit Architecture

The amplifier topology presented in this report is referenced from Hasan & Lee's 2014 paper [2].

Figure 2 illustrates the proposed amplifier architecture, which comprises a first-stage open-loop configuration and a second-stage closed-loop configuration. The circuit block enclosed within the dotted line represents the external high-pass filter and common-mode (CM) biasing, which removes the DC offset caused by the skin-electrode interface. The first stage consists of a rail-to-rail differential amplifier and two voltage buffers. The second stage incorporates a closed-loop class-A amplifier (transistors M_{11} and M_{12}), a voltage buffer, and two gain-enhancement switches (M_9 and M_{10}).

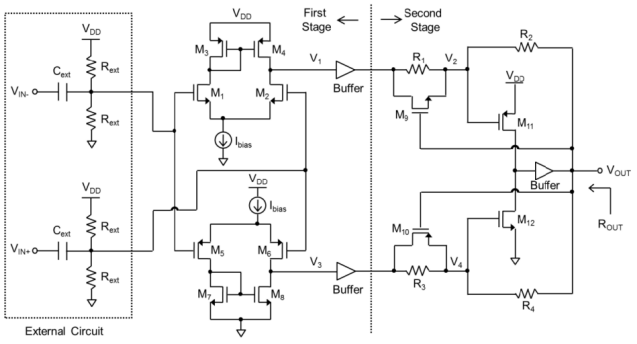

Fig. 2: Schematic architecture of Hasan & Lee's biopotential amplfier.

As depicted in the figure, the first-stage open-loop amplifier is integrated with the second-stage closed-loop amplifier. The NMOS input pair of the first stage drives the PMOS amplifier in the second stage, and vice versa, with the common drains of M_{11} and M_{12} connected to generate the output. This design eliminates the need for separate second-stage amplifiers for the NMOS and PMOS input pairs in the first stage, resulting in a compact amplifier architecture.

The open-loop configuration of the first stage maintains a high input impedance, while the closed-loop configuration of the second stage minimizes overall amplifier gain reduction caused by output level variations. However, due to the closed-loop design, the second-stage input resistance is relatively low, which reduces the gain of the first stage. To address this issue, rail-to-rail voltage buffers are added to the output nodes of the first stage. The schematic of the voltage buffer is shown in Figure 3. An additional buffer is placed at the output node of the second stage to mitigate loading effects, allowing the use of small-size feedback resistors.

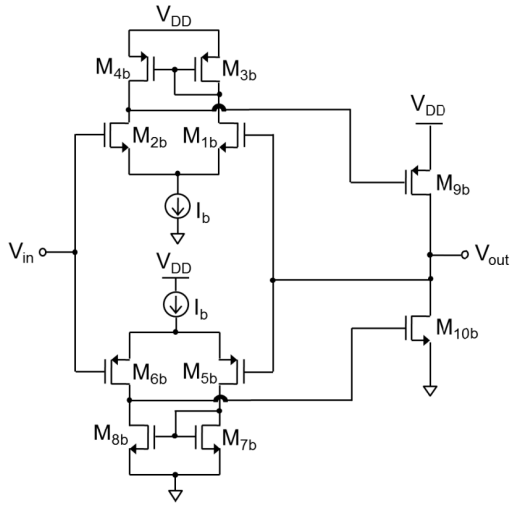

Fig. 3: Schematic of the rail-to-rail voltage buffer with negative feedback.

A. Gain Stages

Assuming matched transconductances, the gain of the NMOS (A_{1n}) and PMOS (A_{1p}) transconductance amplifiers in the first stage can be approximated using the following general formula:

$$A_{1n} = A_{1p} = g_m \left(r_{o,n} \parallel r_{o,p}\right) \tag{1}$$

The second stage open loop gain without the feedback resistors and the gain enhancement switches is:

$$A_2 = -\frac{v_{\text{out}}}{v_2} = -\frac{v_{\text{out}}}{v_4} = g_{m11,12}\left(r_{o11} \parallel r_{o12}\right) \tag{2}$$

Adding in the feedback resistors, the closed-loop gain of the second stage becomes:

$$A_{2,\text{cl}} \approx \frac{\frac{(R_2 \| R_4)}{(R_1 \| R_3)}}{1 + \frac{1}{A_2} \cdot \frac{(R_2 \| R_4)}{(R_1 \| R_3)}} \tag{3}$$

This makes the overall gain of the amplifier:

$$A_{\text{ov}} = A_1 \cdot A_{2,\text{cl}} = \frac{\left(\frac{A_{1n}}{R_1} + \frac{A_{1p}}{R_3}\right)}{\frac{1}{(R_2 \| R_4)} + \frac{1}{A_2} \cdot \left[\frac{1}{(R_1 \| R_2)} + \frac{1}{(R_3 \| R_4)}\right]} \tag{4}$$

Therefore, if $A_2 \gg 1$, A_{ov} will simply be the product of A_1 and the resistor ratios $(R_2 \parallel R_4)/(R_1 \parallel R_3)$. This would work well in the cases where the voltage difference between the inputs $V_{\text{in+}}$ and $V_{\text{in-}}$ is small. However, if $V_{\text{in+}} \gg V_{\text{in-}}$ or $V_{\text{in+}} \ll V_{\text{in-}}$, the output voltage is amplified towards either the V_{DD} or GND rail, causing either M_{11} or M_{12} (respectively) to dip from saturation into triode. Both of these scenarios would cause a gain decrease in A_2, which conflicts with the constant gain over a wide output range design requirement.

The solution is to add feedback using the gain enhancement switches M_9 and M_{10}, where the second stage closed loop gain can now be modeled as:

$$A_{2,\text{cl}} \approx \frac{\frac{(R_2 \| R_4)}{\left(R_1' \| R_3'\right)}}{1 + \frac{1}{A_2} \cdot \frac{(R_2 \| R_4)}{\left(R_1' \| R_3'\right)}} \tag{5}$$

where $R_1' = (R_1 \parallel R_{\text{ON},M9})$ and $R_3' = (R_3 \parallel R_{\text{ON},M10})$. In this scenario, as V_{out} drift toward either V_{DD} or GND, either M_{10} or M_9 will cutoff, causing either R_3' to approach R_3 or R_1' to approach R_1, respectively, since $R_{\text{OFF},M10} \approx R_{\text{OFF},M9} \approx \infty$. In this way, the increase in either R_3' or R_1' compensates for the reduction in A_2.

B. Frequency Response

The lower 3-dB frequency of the proposed amplifier is determined by the external high-pass filter, which removes the electrode offset. Similarly, the upper 3-dB frequency can be adjusted by incorporating additional feedforward capacitors that interact with the first-stage output resistance to create a low-pass filter response. This adjustment is ideally achieved by placing a capacitor at the amplifier's output node. However, due to the low output resistance of the buffer, a large capacitor is required to achieve a low cutoff frequency. Figure 4 illustrates the inclusion of two additional feedforward capacitors, C_{c1} and C_{c2}, located between the first and second stages. These capacitors are positioned at the input of the first-stage buffer to achieve a lower cutoff frequency.

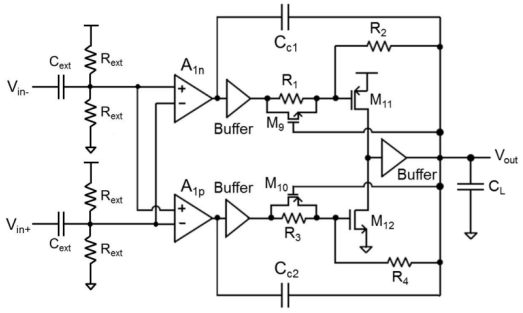

Fig. 4: Simplified schematic showing the feedforward capacitors C_{c1} and C_{c2}.

Taking all of the gain stages into account, the frequency response of the amplifier can be modeled using the following transfer function:

$$H(s) = \frac{A_{\text{hp}} A_1 A_{2,\text{cl}} s \left(1 - \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{\text{php}}}\right)\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \tag{6}$$

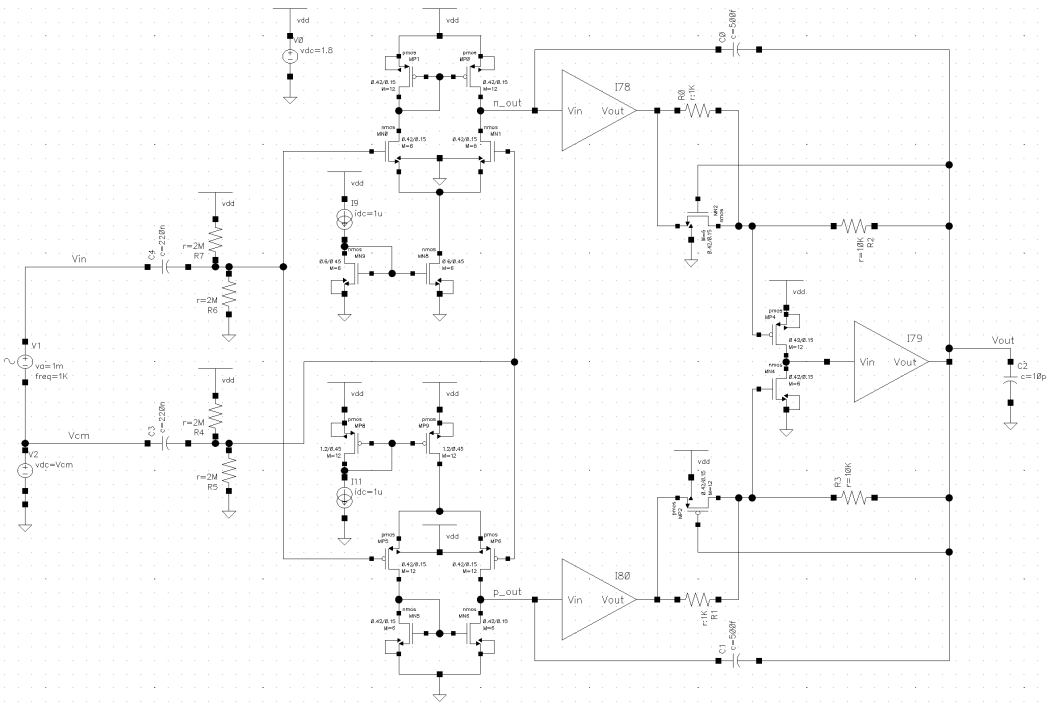

Fig. 5: Cadence implementation of the full amplifier schematic.

Accounting for the Miller effect, the first-stage pole is:

$$\omega_{p1} = \frac{1}{r_{o1} \cdot [C_{o1} + (1 + A_{2,\text{cl}}) \cdot C_c]} \tag{7}$$

The pole formed by the feedforward capacitors can be represented as:

$$\omega_{z1} = \frac{A_2 \cdot R_{2,4}}{C_c R_{\text{buff}} \cdot (R_{1,3} + R_{2,4})} \tag{8}$$

The second stage pole is formed by the load capacitance (C_L) and output resistance (R_{out}), which can be found with the following:

$$\omega_{p2} = \frac{1}{R_{\text{out}} C_L} \tag{9}$$

$$R_{\text{out}} = \frac{R_{\text{buff}}}{1 + \frac{A_2 R_1}{(R_1 + R_2)} + \frac{A_2 R_3}{(R_3 + R_4)}} \tag{10}$$

$$R_{\text{buff}} = \frac{1}{A_{\text{diff}} \cdot (g_{m,b9} + g_{m,b10})} \tag{11}$$

III. Cadence Implementation

The amplifier was implemented in the Cadence Virtuoso design environment as shown in Figures 5 and 6. Current mirrors had to be sized 50% larger than the minumum sizing to minimize early effect mismatch. Low voltage design techniques were used, meaning cascode current mirrors were avoided.

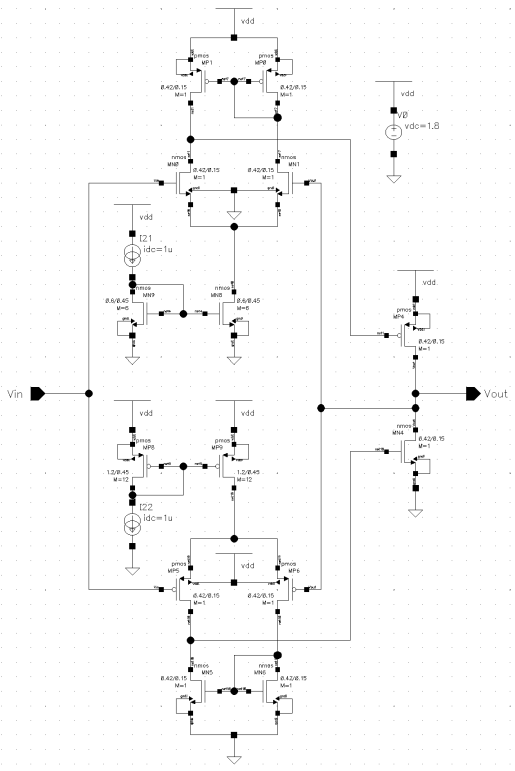

Fig. 6: Cadence implementation of the voltage buffer.

IV. Simulation Results & Discussion

To demonstrate transient operation of the circuit, the circuit was tested with different input common-mode voltages (0V, 900mV, 1.8V). The 900mV common-mode input is shown in

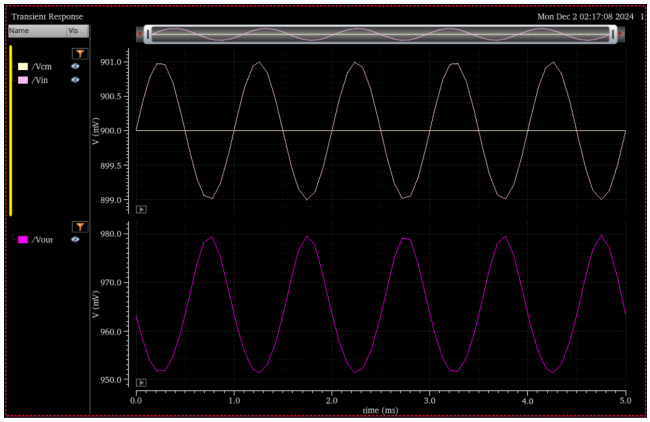

Fig. 7: Transient simulation with 900mV common mode input

Figure 7.

All outputs were the same regardless of common mode input, suggesting that the input DC offset removing high pass filter and the $V_{DD}/2$ resistor biasing are working as intended.

Next, the frequency and phase response of the amplifier was simulated, as shown in Figure 8. The amplifier has a bandwidth

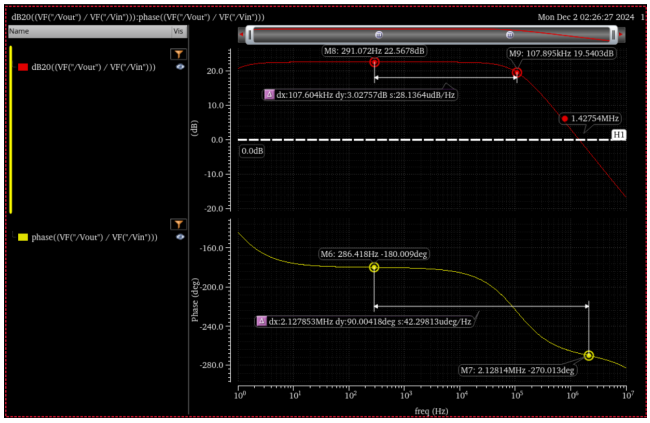

Fig. 8: Amplifier frequency and phase response with upper 3-dB frequency cutoff ($f_{3\text{dB}}$) and unity gain frequency labeled (f_{UN}).

of 100kHz with ∼22.5dB of constant differential gain. This gain is easily adjustable with the internal feedback resistors. The initial phase response of the amplifier is due to the external high pass filter. As demonstrated in Figure 8, when the phase reaches -90 degrees off nominal (inverting is -180 degrees phase), the gain is already below unity, meaning the circuit is stable since high frequency noise is attenuated. The >45 degree phase margin was enabled due to the careful tuning of the upper cutoff frequency (f_{3dB}), which is determined by the feedforward coupling capacitors C_{c1} and C_{c2}.

The common mode frequency gain response of the amplifier was tested in Figure 9, showing a consistent -40dB common mode gain throughout the frequency bandwidth of the amplifier. This correlates to a common-mode rejection ratio (CMRR) of about 62.6dB. This value is easily adjustable with the internal feedback resistors.

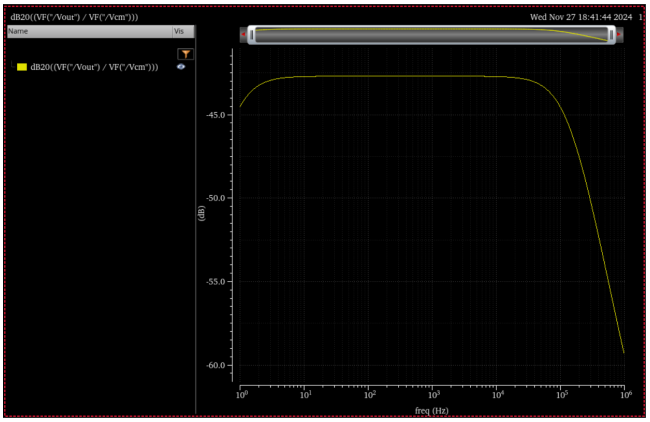

Fig. 9: Common mode frequency gain response showing high CMR.

A differential voltage sweep was also performed in Figure 10 at the input in order to approximately determine the input and output linear voltage range. This was done without the external high pass filter to allow for a DC analysis. The maximum differential input and output voltages were

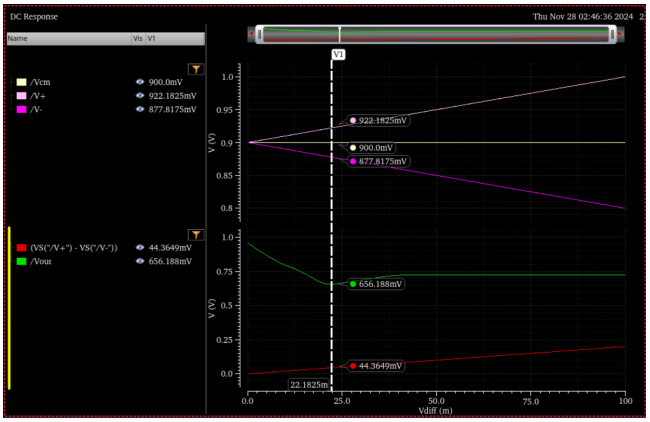

Fig. 10: Output response of the amplifier following a differential DC sweep of the amplifier input.

determined by sweeping the positive and negative inputs away from a $V_{DD}/2$ commmon-mode voltage in their respective directions until non-linear behavior is visible at the output. Using this technique, the differential input voltage range was found to be around 44 mV (a sufficient margin above typical biopotential signal amplitudes), and the output voltage range was found to be around 600mV (calculated after applying 22.5dB of gain to the input).

REFERENCES

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